GSM and DCS SiGe BiCMOS Mixer ICs with Wide LO Power Range

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Abstract — **GSM and DCS mixer ICs operating with the LO drive ranging from –35 dBm to –5 dBm and the supply voltage ranging from 2.4 V to 3.6 V are reported in this paper. The measured conversion gain and noise figure of the GSM mixer are 8.9 dB and 10.2 dB, respectively, and those of the DCS mixer are 8.5 dB and 10.9 dB. The GSM mixer IIP3 is 1 dBm, whereas the DCS mixer IIP3 is 4 dBm. A high-gain multistage LO driver and bias currents insensitive to supply voltage variation facilitate the mixer application for commercial mobile terminals. The GSM and DCS mixers were designed and fabricated using 0.25-μm SiGe BiCMOS process. An integrated GSM (DCS) mixer, comprising a Gilbert core, an LO driver, a limiter, an IF buffer and bias circuits, consumes 28.5 mA from a 3-V battery. The SiGe BiCMOS mixers feature comparable IIP3, higher gain, and lower noise figure than do our previously fabricated Si BiCMOS mixers based on the same topology, and also consume 29% less power.**

I. Introduction

The demand for low-power, fully integrated wireless receivers has placed higher performance requirements on the receive mixer design. The suitability of SiGe for low power mixers has been reported in [1]. Several mixers for commercial cellular applications have been reported [2,3]. The performance of commercial mixers is dependent on the fluctuation of the VCO power. The mixer should be designed so that its conversion gain, noise figure and linearity remain constant for a wide range of the LO drive. This work addresses the stability of mixer operation for the LO signal ranging from –35 dBm to –5 dBm, which is achieved using a four-stage LO buffer and a limiter.

A commercial mixer must be operable with a single supply voltage and bias circuits must be generated on-chip. The mixer bias condition should remain steady for a wide temperature range and be insensitive to processing parameter and bias supply variations. This paper presents a mixer with internally generated bias circuitry, designed to operate over the temperature range from –30 °C to +90 °C and to tolerate supply voltage variation and fabrication mismatches of ±20% from their respective nominal values. The design of the bias circuit is presented in detail in Section 2.

II. Circuit Design

The topology of the GSM and DCS mixers is identical, but the values of the passive and active components differ. Fig. 1 shows the block diagram of the integrated mixer consisting of a Gilbert core, LO driver, limiter, IF buffer and bias and control circuits.

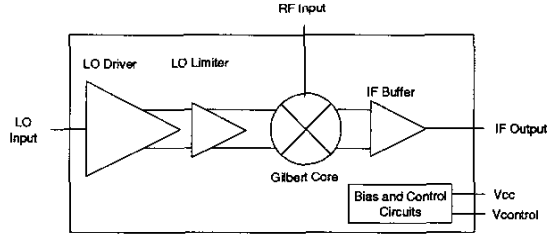

Fig. 1. Mixer IC Block Schematic.

The Gilbert core, LO limiter and IF buffer are depicted in Fig. 2. The Gilbert core and limiter employ NMOS switches (transistors M1, M2 and M3), which define the mixer's state of operation (on/off). The option to switch off a mixer facilitates downconversion using the DCS and the GSM mixer in a dual-mode receiver. The RF transconductor is realized as a common-emitter stage because of its superior linearity in comparison to a common-base transconductor.

The LO limiter shapes the LO drive, approximating ideal LO switching. The Gilbert core output is buffered to provide impedance matching. The LO driver (Fig. 3) is designed as a combination of differential non-degenerated common-emitter gain and emitter-follower buffer stages. The latter reduces the loading of the former and

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maximizes the driver bandwidth. The LO buffer comprises two differential common-emitter and two differential common-collector stages.

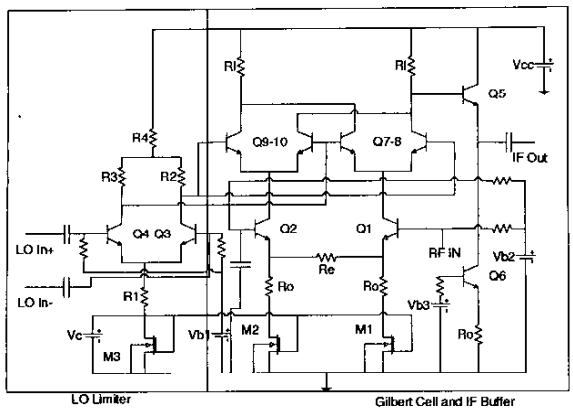

Fig. 2. Gilbert Core, LO Limiter and IF Buffer Schematic.

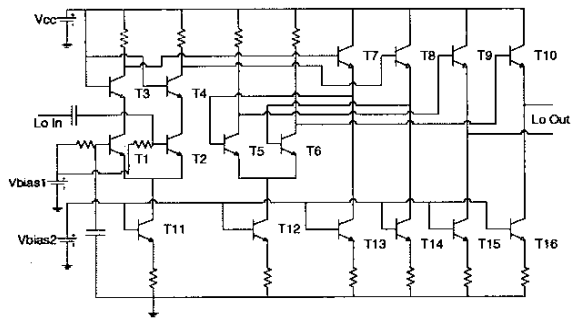

Fig. 3. LO Driver Schematic.

The input stage of the LO driver (transistors T1, T2, T3 and T4) is differential cascode to provide superior isolation between the LO driver output and input. It also converts a single-ended VCO output to a fully differential signal. The gain of the LO driver exceeds 25 dB and enables the mixer operation for the input LO signal as low as –35 dBm. Large input and output transistors have been used to provide protection against electrostatic discharges (ESD).

The bias circuit is depicted in Fig. 4. Reference voltages V_{REF} are applied to the Gilbert core, LO driver, limiter and IF buffer to provide bias independent of temperature changes and voltage supply ripples. Transistors (Q_1, Q_2) and resistors (R_4, R_5) comprise a Nagata current mirror [4] and guarantee the insensitivity of I_2 to Vcc variation. Assuming that the collector currents of Q_1 and Q_2 are I_1 and I_2, respectively, and ignoring the basewidth modulation, the following relationship can be established:

$$aI_1 e^{-\frac{R_5 I_1}{V_T}} = I_2 e^{\frac{R_4 I_2}{V_T}} \qquad (1)$$

where V_T is the thermal voltage and a is the ratio between Q_2 and Q_1 emitter areas.

Assuming that M_1 operates in the linear region and that its overhead voltage is negligible, the following relationship can be established between the supply voltage Vcc and current I_1:

$$R_6 I_1 + V_{BE1} = V_{CC} \qquad (2)$$

where $V_{BE1} = V_T \ln\left(\frac{I_1}{I_{S1}}\right)$ is the Q_1 base-emitter junction voltage. From the relationships (1) and (2) it could be inferred that I_1 will rise with the increase of V_{CC}. The left side of the equation (1) is a product of a linear and a negative exponential term, whereas the right side is a product of a linear and a positive exponential term. If the value of I_1 is within a range in which the exponential and the linear term have comparable contributions, the left-side product will not significantly fluctuate, and so the value of I_2 will be bounded. Consequently, the voltage supply variation will not impact I_2 significantly, even though the value of I_1 varies.

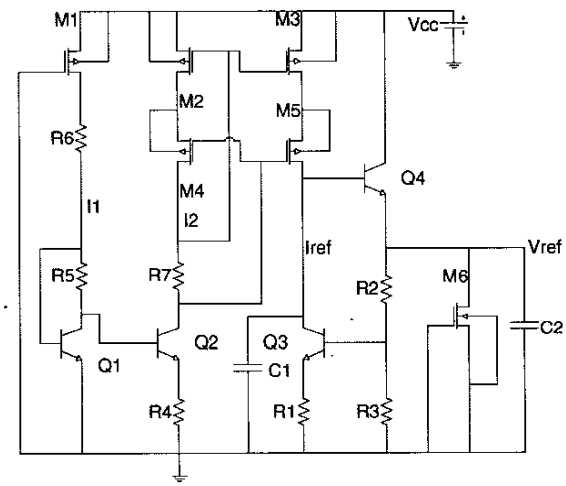

Fig. 4. Bias Circuit Schematic.

Transistors M_4 and M_5 compensate the channel modulation effect and together with the current mirror (M_2,M_3) guarantee that I_{REF} is proportional to I_2, and so I_{REF} will be bounded if Vcc varies. The reference voltage V_{REF}:

$$V_{REF} = (1 + R_2 / R_3)(V_{BE3} + I_{REF} R_1) \qquad (3)$$

is independent of supply voltage ripples, since I_{REF} and base-emitter junction voltage V_{BE3} vary insignificantly with Vcc. The thermal change of the bias voltage and current can be minimized by careful selection of R_1 and R_2/R_3. The reference voltage in the bias circuit is also independent of fabrication mismatches of over ±20% from the nominal values of the circuit components.

III. Technology

The GSM and DCS mixers were designed and fabricated using a SiGe BiCMOS process that features 0.25-μm CMOS transistors for 2.5-V operation. This process yields SiGe HBTs with 60 GHz f_{MAX}, two types of polysilicon resistors, nitride capacitors and three aluminum metal layers. The technology is described in more detail elsewhere [5].

IV. Measurement Results

The GSM integrated mixer micrograph is shown in Fig. 5. The topologies of the GSM and DCS mixers are the same and so are the corresponding layouts similar.

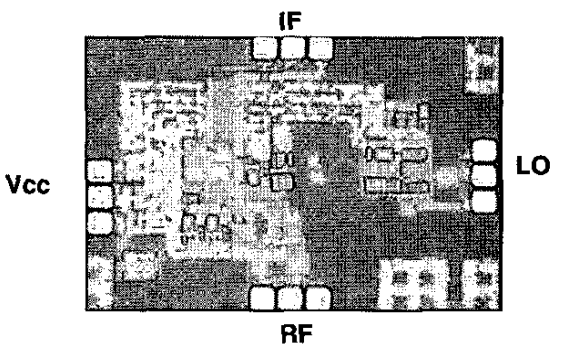

Fig. 5. Mixer Micrograph.

The die size is 1.7 x 1.3 mm^2. For measurement purposes, the RF, LO and IF ports are single-ended. Both GSM and DCS mixer operate with the upper-side LO injection and the IF frequency of 130 MHz. They draw 28.5 mA from a 3-V supply, consuming 85.5 mW. The previously fabricated Si BiCMOS mixers using the same topology as SiGe BiCMOS mixers have lower gain, higher noise figure, and comparable IIP3 to those of the SiGe BiCMOS mixers and consume 40 mA from a 3-V battery. The variation of the SiGe mixers' DC current with respect to supply voltage Vcc is depicted in Fig. 6. This figure shows that by careful design of bias circuits, DC current fluctuation resulting from voltage ripples can be minimized.

The GSM and DCS mixer conversion gains are 8.9 dB and 8.5 dB respectively, and the corresponding double-side band (DSB) noise figures are 10.2 dB and 10.9 dB. The GSM and DCS mixer measurement results are summarized in Table 1. The GSM and DCS mixer conversion gain and noise figure deviate less than 10% (in dBs) from their nominal values as the supply voltage Vcc is swept from 2.5 to 3.6 V. The mixers gain and noise figure dependence on Vcc is depicted in Fig. 7. As shown in Fig. 8, the mixers operate with the LO drive higher than –35 dBm. The mixers robustness is proved by congruence between simulated and measured results, despite a significant deviation of fabricated resistor sheet density and bipolar transistor h_{FE} from the simulation parameters. The thermal simulation shows a change of less than 10% for the mixers conversion gain, noise figure and third-order input intercept (IIP3) across the temperature range from -30 °C to 90 °C.

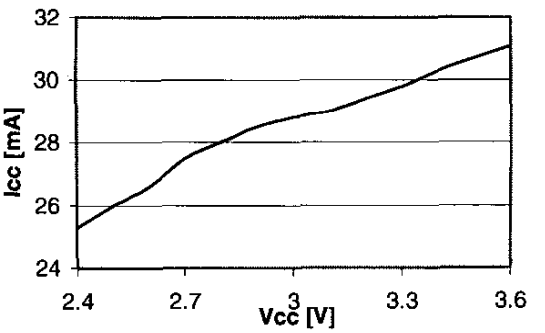

Fig. 6. DC Current vs. Supply Voltage Vcc.

	GSM Mixer	DCS Mixer
RF Frequency [MHz]	900 MHz	1800 MHz
Conversion Gain [dB]	8.9	8.5
DSB Noise Figure [dB]	10.2	10.9
Third-Order Input Intercept [dBm]	1	4
Supply Current [mA]	28.5	28.5
LO Power [dBm]	–35 to –5	–35 to –5

Table 1. Integrated Mixers Performance Summary.

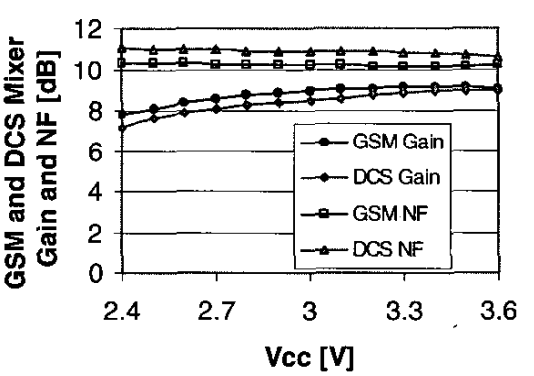

Fig. 7. Gain and Noise Figure vs. Vcc.

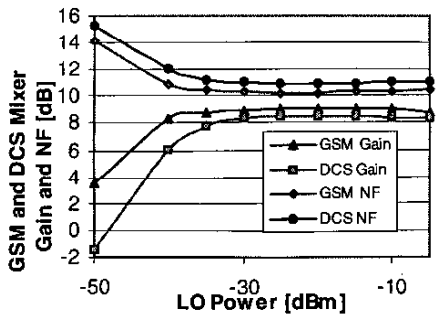

Fig. 8. Gain and Noise Figure vs. LO Power.

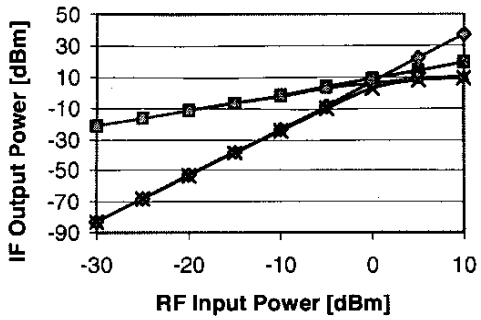

Fig. 9. GSM Mixer Fundamental and Third Harmonic Output IF Power vs. RF Input Power.

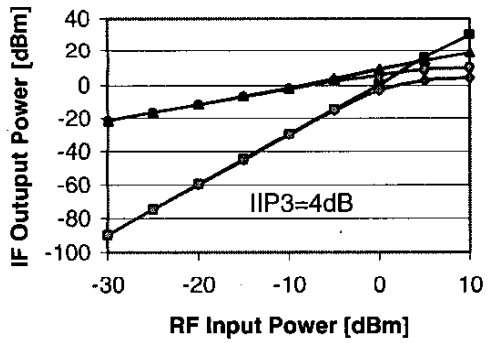

Fig. 10. DCS Mixer Fundamental and Third Harmonic Output IF Power vs. RF Input Power.

The output power of the GSM and DCS mixer's fundamental and third harmonic as a function of RF input power is shown in Fig. 9 and Fig. 10, respectively. The intercept point of the fundamental and third harmonic lines denotes IIP3 and OIP3, which values are 4 dBm and 12.5 dBm, respectively, for the DCS mixer, and 1 dBm and 10 dBm for the GSM mixer.

V. Conclusion

Integrated GSM and DCS mixers operable for the LO drive ranging from –35 dBm to –5 dBm have been presented. The performance of the mixers changes insignificantly as the supply voltage Vcc is swept from 2.4 to 3.6 V. The measured GSM mixer conversion gain and noise figure are 8.9 dB and 10.2 dB, respectively, and those of the DCS mixer are 8.5 dB and 10.9 dB. Each mixer was fabricated using 0.25 μm SiGe BiCMOS process with 60-GHz HBTs, consuming 28.5 mA from a 3-V battery. The SiGe BiCMOS mixers have comparable IIP3, higher gain, and lower noise figure than our previously fabricated Si BiCMOS mixers with the same circuit topology, yet they consume 29% percent less power. The SiGe mixers meet the requirements for GSM and DCS commercial mobile terminals. Their switching capability facilitates their combination in a dual-mode receiver.

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